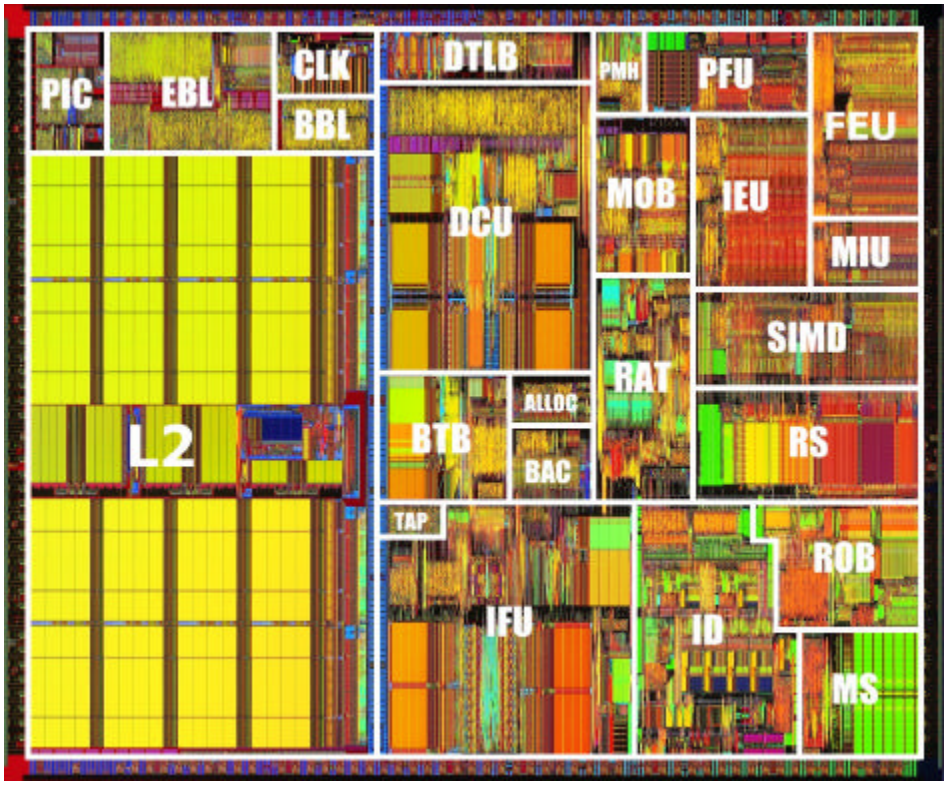
Pentium® III Processor die photo fact sheet



Statistics

0.18 micron 6-layer metal CMOS process technology
28.1M transistors
106 mm die size (normalized)
3-way superscalar out-of-order execution micro-architecture
256K Level 2 Cache
133 MHz IO bus

Bottom center region

Logic for the front-end of the pipeline resides here.

IFU Instruction Fetch Unit. Instruction fetch logic and a 16K Byte 4-way set-associative level one instruction cache resides in this block. Instruction data from the IFU is then forwarded to the ID.

BTB Branch Target Buffer. This block is responsible for dynamic branch prediction based on the history of past branch decisions paths.

BAC Branch Address Calculator. Static branch prediction is performed here to handle the BTB miss case.

TAP Testability Access Port. Various testability and debug mechanisms reside within this block.

Bottom right region

Instruction decode, scheduling, dispatch, and retirement functionality is contained within this region.

ID Instruction Decoder. This unit is capable of decoding up to 3 instructions per cycle.

MS Micro-instruction Sequencer. This holds the microcode ROM and sequencer for more complex instruction flows. The microcode update functionality is also located here.

RS Reservation Station. Micro-instructions and source data are held here for scheduling and dispatch to the execution ports. Dispatch can happen out-of-order and is dependent on source data availability and an available execution port.

ROB Re-Order Buffer. This supports a 40-entry physical register file that holds temporary write-back results that can complete out of order. These results are then committed to a separate architectural register file during in-order retirement.

Top right region

This primarily consists of the execution datapath for the Pentium® III processor.

SIMD SIMD integer execution unit for MMX™ Technology instructions.

MIU Memory Interface Unit. This is responsible for data conversion and formatting for floating point data types.

IEU Integer Execution Unit. This is responsible for ALU functionality of scalar integer instructions. Address calculations for memory referencing instructions are also performed here along with target address calculations for jump related instructions.

FEU Floating point Execution Unit. This performs floating point related calculations for both existing scalar instructions along with support for some of the new SIMD-FP instructions.

PFU Packed Floating point arithmetic Unit. This contains arithmetic execution data-path functionality for SIMD-FP specific instructions.

Top center region

Functionality in this region is split into assorted functions including data cache access, and allocation.

ALLOC Allocator. Allocation of various resources such as ROB, MOB, and RS entries is performed here prior to micro-instruction dispatch by the RS.

RAT Register Alias Table. During resource allocation the renaming of logical to physical registers is performed here.

MOB Memory Order Buffer. Acts as a separate schedule and dispatch engine for data loads and stores. Also temporarily holds the state of outstanding loads and stores from dispatch until completion.

DTLB Data Translation Look-aside Buffer. Performs the translation from linear addresses to physical address required for support of virtual memory.

PMH Page Miss Handler. Hardware engine for performing a page table walk in the event of a TLB miss.

DCU Data Cache Unit. Contains the non-blocking 16K Byte 4-way set-associative level one data cache along with associated fill and write back buffering.

Left region

Functionality in this area includes bus interface circuitry and a level 2 cache.

BBL Back-side Bus Logic. Logic for interface to the back-side bus for accesses to the internal unified level two processor cache.

EBL External Bus Logic. Logic for interface to the external front-side bus.

PIC Programmable Interrupt Controller. Local interrupt controller logic for multi-processor interrupt distribution and boot-up communication.

CLK Clocking. Contains phase lock loop and other clocking control circuitry.

L2 Level 2 Cache. 256K unified level two cache.